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09/921,554	08/06/2001	Masahito Matsuo	027260-482	7038

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,554	MATSUO, MASAHITO	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5,7,8 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5,7,8 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been examined.

Papers Received

2. Receipt is acknowledged of the amendment papers, where the papers have been placed of record in the file.

3. The Examiner thanks Applicant for correcting informalities throughout the specification.

4. The objections to the claims and many of the 35 USC 112 rejections of the claims have been overcome by the amendment and are herein withdrawn.

5. The objection to the title and 35 USC 112 rejections to claims 3 and 5 have been maintained as given below. Applicant does not appear to have addressed these 35 USC 112 issues by amendment or remark.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The amended title does not give a clear indication of the invention itself, but only gives an indication of the art the invention is a part of.

The following title is suggested: Data Processor Speeding Up Repeat Processing By Inhibiting Remaining Instructions After A Break In A Repeat Block.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 3 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 3 is very unclear as to how the instruction processing sequence switches to a next instruction of the repeat block when the claim has specifically stated that remaining instructions of the repeat block are inhibited from being executed. The examiner is taking the claim to mean that the execute stage processes remaining instructions in the pipeline after a break but converts them to NOPs before switching to these NOPs, thus effectively inhibiting the original instruction from being executed as taught in the specification. The Examiner notes that this NOP is not the next instruction of the repeat block, but is a substitute instruction.

10. Claim 5 is very unclear as to how one would jump to a next instruction in a block of instructions when the current instruction is a last instruction that is executed last in the block. In such a case there would be no next instruction in the block. The Examiner is taking the claim to mean that upon reaching the end of a repeat block, the next instruction to be executed is jumped to.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 3, 5, 7, 8, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato (6,345,357).

13. In regard to claim 3, Sato discloses a data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly (column 15, line 62 – column 16, line 47 show an embodiment using both step-repeat and block-repeat processing with details discussed prior in the document), said data processor comprising:

a. detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; [Column 12, line 63 – column 13, line 18 show that a repeat end flag is detected and indicates that the number of repeats is completed and thus the repeat block is broken. This is shown to have no dependencies on the actual operation being executed anywhere in the disclosure.]

b. and instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit the execution of the remaining instructions in said repeat block, [As shown in column 12, line 63 – column 13, line 18, after detecting this repeat end flag, remaining instructions in the repeat block are negated or set to NOP and effectively inhibited. This is further shown in column 13, line 65 - column 14, line 18 with

figures 11-12 that illustrate that remaining instructions N+8 to N+11 in a repeat block are converted to NOPs and thus inhibited.]

c. wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to a next instruction of said repeat block at an instruction fetch stage upon detection of said break of said repeat processing by said detecting means. [Column 13, line 65 - column 14, line 18 shows that the next instruction after the break is fetched.]

14. In regard to claim 5, Sato discloses a data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly (column 15, line 62 – column 16, line 47 show an embodiment using both step-repeat and block-repeat processing with details discussed prior in the document), said data processor comprising:

a. detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; [Column 12, line 63 – column 13, line 18 show that a repeat end flag is detected and indicates that the number of repeats is completed and thus the repeat block is broken. This is shown to have no dependencies on the actual operation being executed anywhere in the disclosure.]

b. and instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit the execution

of the remaining instructions in said repeat block, [As shown in column 12, line 63 – column 13, line 18, after detecting this repeat end flag, remaining instructions in the repeat block are negated or set to NOP and effectively inhibited. This is further shown in column 13, line 65 - column 14, line 18 with figures 11-12 that illustrate that remaining instructions N+8 to N+11 in a repeat block are converted to NOPs and thus inhibited.]

c. wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to the next instruction of said repeat block at an instruction fetch stage upon detection of said break of said repeat processing by said detecting means. [Column 13, line 65 - column 14, line 18 shows that the next instruction after the break is fetched.]

d. wherein said instruction processing sequence switching means is means for performing jump processing to the next instruction of said repeat block during execution of a last instruction that is executed last in said repeat processing of said repeat block. [Column 7, line 64 – column 8, line 9 show that the last instruction in a repeat block is detected and the starting address of the block (SRPT_S) is transferred over the JA (jump address) bus. Column 8, lines 20-26 show that the first address of the repeat block is jumped to in the execution stage. This is also illustrated in column 10, lines 50-61. Further, the included dictionary definition of "jump", as it pertains to computer science (definition 9), states that to jump (and thus to perform jump processing) is simply to move from

one set of instructions in a program to another out of sequence. Thus when Sato discloses returning to the first instruction in the repeat block (which is out of sequence from the last instruction), as indicated by Applicant, Sato is also disclosing jumping and since a processor is disclosed, jump processing.]

15. In regard to claim 7, Sato discloses a data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly (column 15, line 62 – column 16, line 47 show an embodiment using both step-repeat and block-repeat processing with details discussed prior in the document), said data processor comprising:

a. detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; [Column 12, line 63 – column 13, line 18 show that a repeat end flag is detected and indicates that the number of repeats is completed and thus the repeat block is broken. This is shown to have no dependencies on the actual operation being executed anywhere in the disclosure.]

b. and instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit the execution of the remaining instructions in said repeat block, [As shown in column 12, line 63 – column 13, line 18, after detecting this repeat end flag, remaining instructions in the repeat block are negated or set to NOP and effectively inhibited. This is further shown in column 13, line 65 - column 14, line 18 with

figures 11-12 that illustrate that remaining instructions N+8 to N+11 in a repeat block are converted to NOPs and thus inhibited.]

c. wherein said detecting means is means for deciding whether said repeat processing breaks, based on an address of an instruction that is executed during said repeat processing of said repeat block. [Column 10, lines 50-61 show that if the last instruction is detected and the counter is still above 1, control is changed over (to the beginning of the repeated section), and thus a break is not set forth, effectively showing a break would be set forth in the case where the counter was at 0. This is indeed shown to be the case in column 12, line 63 – column 13, line 18 that the counter at zero signifies a break in repeat processing.]

16. In regard to claim 8, Sato discloses the data processor according to claim 7, wherein said detecting means has count means for counting a number of repetitions of processing of said repeat block, and comparison means for comparing the address of the instruction to be currently processed in said repeat block with the address of a last instruction to be executed last in said repeat processing of said repeat block, and wherein upon being informed from said comparison means of the coincidence of address between said instruction to be currently processed and said last instruction when the count number of said count means has reached a predetermined value, said detecting means decides that said repeat processing breaks (as shown above).

17. In regard to claim 11, Sato discloses a data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly (column 15, line 62 – column 16, line 47 show an embodiment using both step-repeat

and block-repeat processing with details discussed prior in the document), said data processor comprising:

a. detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; [Column 12, line 63 – column 13, line 18 show that a repeat end flag is detected and indicates that the number of repeats is completed and thus the repeat block is broken. This is shown to have no dependencies on the actual operation being executed anywhere in the disclosure.]

b. and instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit the execution of the remaining instructions in said repeat block, [As shown in column 12, line 63 – column 13, line 18, after detecting this repeat end flag, remaining instructions in the repeat block are negated or set to NOP and effectively inhibited. This is further shown in column 13, line 65 - column 14, line 18 with figures 11-12 that illustrate that remaining instructions N+8 to N+11 in a repeat block are converted to NOPs and thus inhibited.]

c. wherein said detecting means is means for deciding whether said repeat processing breaks, based on an address of an instruction that is executed during said repeat processing of said repeat block. [Column 10, lines 50-61 show that if the last instruction is detected and the counter is still above 1, control is changed over (to the beginning of the repeated section), and thus a break is not set forth,

effectively showing a break would be set forth in the case where the counter was at 0. This is indeed shown to be the case in column 12, line 63 – column 13, line 18 that the counter at zero signifies a break in repeat processing.]

d. wherein said detecting means has first count means for counting a number of repetitions of processing of said repeat block and second count means for counting the number of instructions executed during each repeat processing of said repeat block, and said detecting means decides that said repeat processing breaks when a count number of said first count means reaches a first predetermined value and the count number of said second count means reaches a second predetermined value in a last repeat processing of said repeat block. [As shown above, the counter down counts the number of instructions to be executed in a repeat block and breaks at a predetermined value 0. As shown in column 15, line 62 – column 16, line 47, a register or counter also tracks repeat block iterations in the same manner and looks for predetermined value 0. When one of these counters reaches 0, in response the repeat processing breaks as indicated previously. At this time, the other counter is inherently at some other value, which is predetermined since the value is inherently determined before the break takes place.]

Response to Arguments

18. Applicant's arguments filed 10/27/04 have been fully considered but they are not persuasive.

19. Applicant has argued with respect to claim 3 (with reference to the example of figure 12 of Sato) that instructions N+8 to N+12 are all fetched abut not executed (due to NOP) in Sato, whereas the invention would not fetch nor execute the instructions. The Examiner respectfully submits that claim 3 does not claim inhibiting fetching but only execution, which as indicated by Applicant, Sato discloses.

20. Applicant has argued in regard to claim 5 that Sato does not disclose performing jump processing to the next instruction of the repeat block, but instead discloses *returning* to the first instruction in the repeat block during repeat processing. The included dictionary definition of "jump", as it pertains to computer science (definition 9), states that to jump (and thus to perform jump processing) is simply to move from one set of instructions in a program to another out of sequence. Thus when Sato discloses returning to the first instruction in the repeat block (which is out of sequence from the last instruction), as indicated by Applicant, Sato is also disclosing jumping and since a processor is disclosed, jump processing. Further, column 7, line 64 – column 8, line 9 show that the last instruction in a repeat block is detected and the starting address of the block (SRPT_S) is transferred over the JA (jump address) bus. Column 8, lines 20-26 show that the first address of the repeat block is jumped to in the execution stage. This is also illustrated in column 10, lines 50-61.]

21. Applicant has argued with respect to claim 7 that in Sato the end of the repeat is determined by the number of instructions performed in the repeat processing, whereas the claim decides when to break based on an address of an instruction that is executed during repeat processing in addition to the address of the last instruction in repeat

processing. The Examiner respectfully submits that nowhere in claim 7 is a break detected based on the address of the last instruction in repeat processing, but it is only claimed that a break is detected based on an address of an instruction that is executed during said repeat processing. Column 10, lines 50-61 show that if the last instruction is detected and the counter is still above 1, control is changed over (to the beginning of the repeated section), and thus a break is not set forth, effectively showing a break would be set forth in the case where the counter was at 0. This is indeed shown to be the case in column 12, line 63 – column 13, line 18 that the counter at zero signifies a break in repeat processing. The included IEEE definition of "address" shows that an address may be interpreted as an identification, as represented by a number, for any data source or destination. Thus the counter provides a number or identification for other registers (data sources and destinations) holding value to compare to (as given in the sections above). Also, as shown in these sections, the counter is of an instruction (in fact all the instructions) executed in the repeat block since the counter keeps track of the iterations of execution.]

22. Applicant has argued with respect to claim 11 that Sato does not teach determining a break based upon two different counters. As shown above, the counter down counts the number of instructions to be executed in a repeat block and breaks at a predetermined value 0. As shown in column 15, line 62 – column 16, line 47, a register or counter also tracks repeat block iterations in the same manner and looks for predetermined value 0. When one of these counters reaches 0, the repeat processing breaks as indicated previously. At this time, the other counter is inherently at some

other value, which is predetermined since the value is inherently determined before the break takes place.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
January 19, 2005

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